C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: - Electronics & Communication Engineering
SEMESTER: - I **CODE**: - 5TE01CVD1
NAME – CMOS VLSI Design (CVD)

Teaching & Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE01CVD1	CMOS VLSI Design (CVD)	03	00	02	05	04	30	1.5	70	3.0	---	20	30	150

Objectives: -

- In this course, student will study MOS Transistor operation and limitations, MOS digital logic circuits (NMOS & CMOS), the fundamental concepts and structures of designing digital VLSI systems include CMOS devices and circuits, standard CMOS fabrication processes, static &dynamic logic, combinational and sequential circuits, propagation delay, transistor sizing, MOS IC fabrication, layout and design rules, stick diagrams.

Prerequisites: Students enrolled in this course are expected to have an undergraduate-level equivalent background in the following topics: Logic Circuit Design, Microelectronics, MOSFET Operation, MOS-based Logic gates, Sequential Circuits, Fundamental programming skills.

Course Outlines:-

Sr. No.	Course Contents
1	**Introduction To CMOS Circuits** MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, CMOS and nMOS Comparison.
2	**MOS Transistor Theory** Introduction MOS Device Design Equations, The Complementary CMOS Inverter-DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate- DC Characteristics, The Tri State Inverter, Latch up.
3	**Circuit Characterization and Performance Estimation** Resistance Estimation Capacitance Estimation, Switching Characteristics CMOS-Gate Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing
4	**CMOS Circuit And Logic Design** CMOS Logic Gate Design, Basic Physical Design of Simple Gate, CMOS Logic Structures, Clocking Strategies, I/O Structures, Low Power Design.
5	**Design for Testability** Introduction, Faults Models, Ad Hoc Testing, Scan Design, Structured Design for testability, Built-In Self-Test (BIST), IDDQ Testing.
6	**CMOS Sub System Design** Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements.

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Learning Outcomes: -

- To be able to use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnect.
- To be able to create models of moderately sized CMOS circuits that realize specified digital functions.
- To be able to apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
- Have an understanding of the characteristics of CMOS circuit construction and the comparison between different state-of-the-art CMOS technologies.

Books Recommended:-

1. Neil. H.E. Weste and K. Eshragian, "Principles of CMOS VLSI Design". 2nd Edition. Addison-Wesley , 2000.
2. Douglas a. Pucknell and K. Eshragian., "Basic VLSI Design" 3rd Edition. PHI, 2000.
3. R. Jacob Baker, Harry W. LI., & David K. Boyce., "CMOS Circuit Design", 3rd Indian reprint, PHI, 2000.

Research Reference:-

1. International Journal of Advanced Research in Computer Science and Electronics Engineering (IJARCSEE),ISSN: 2277 – 9043
2. Applicable Algebra in Engineering, Communication and Computing, ISSN: 0938-1279,1432-0622
3. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
4. Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on
5. Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
6. Solid-State Circuits, IEEE Journal

C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: - Electronics & Communication Engineering
SEMESTER: - I **CODE**: - 5TE01ENC1
NAME – Embedded Network and Controllers (ENC)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE01ENC1	Embedded Network and Controllers (ENC)	04	00	02	06	05	30	1.5	70	3.0	---	20	30	150

Objectives: -

- The objective of the subject is to provide detailed knowledge on basics of embedded networking and different types of communication protocols and devices used in networking of embedded systems.

Prerequisites: Basic knowledge of Computer networks and protocols are necessary.

Course Outlines: -

Sr. No.	Course Contents
1	**Understanding Embedded Networking Requirements:** Embedded Networking for Beginners, Code Requirements for Embedded Systems, Communication Requirements for Embedded Networking
2	**Devices and Communication Buses for Device Network:** I/O Types and Examples, Serial Communication Devices, Parallel Device Ports, Sophisticated Interfacing Features in Device Ports, Networked Embedded Systems, Serial Bus Communication Protocol, Parallel Bus Device Protocols – Parallel Communication Network using ISA, PCI, PCI-X and Advanced Buses
3	**The I2C Bus:** The Master/Slave Concept in I2C, The I2C Data Format, A Few Words about Addressing, A Typical I2C Bus Configuration, Extension to the Basic Concept
4	**Universal Serial Bus (USB):** Speed Identification on the Bus, USB States, USB Bus Communication, Descriptors
5	**Controller Area Network (CAN):** General Overview, CAN Versions, Bus States, Message Coding, Frames, Priority and Arbitration, Error Detection and Handling, Synchronization and Bit Stuffing, Bit Timing, Physical Layers and Media, Higher Layer Protocols, PIC18FXX8 Family Microcontrollers with CAN Module
6	**Embedded Ethernet:** Elements of a Network, Inside Ethernet, Building a Network: Hardware Options – Cables, Connections and Network Speed, Design Choices – Ethernet Controllers, Using the Internet Protocol in Local and Internet Communications – Connecting to the Internet, Exchanging Messages using UDP and TCP – Basic Communications

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Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand the basics of embedded networking.
- Understand different communication protocols used in internetworking of embedded systems.
- Understand network controllers used in embedded systems.

Books Recommended:-

1. "Embedded Networking with CAN and CANopen", **Olaf Pfeiffer, Andrew Ayre and Christian Keydel**, Copperhill Technologies Corporation
2. "Embedded Systems – Architecture, Programming and Design", **Raj Kamal**, McGraw Hill
3. "Designing Embedded Internet Devices", **Dan Eisenreich and Brian DeMuth**, Elsevier
4. "Embedded Ethernet and Internet Complete", **Jan Axelson**, Lakeview Research
5. "Advanced PIC Microcontroller Projects in C", **Dogan Ibrahim**, Elsevier
6. "PIC18FXX8 Datashets", Microchip

C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: -Electronics & Communication Engineering
SEMESTER: - I **CODE**: - 5TE01EMD1
NAME – Embedded System Design (EMD)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE01EMD1	Embedded System Design (EMD)	04	00	02	06	05	30	1.5	70	3.0	---	20	30	150

Objectives: -

- The objective of the subject is to provide fundamental knowledge of embedded systems and their core components such as hardware and software, as well as steps and issues in designing an embedded system along with real world examples.

Prerequisites: Basic knowledge of Microprocessor, Mircocontroller and programming is necessary.

Course Outlines: -

Sr. No.	Course Contents
1	**Introduction to Embedded Systems:** Embedded Systems, Processor Embedded into a System, Embedded Hardware Units and Devices in a System, Embedded Software in a System, Examples of Embedded Systems, Embedded System-on-Chip (SoC) and Use of VLSI Circuit Design Technology, Complex System Design and Processors, Design Process in Embedded Systems, Formalization of System Design, Design Process and Design Examples, Classification of Embedded Systems, Skills Required for an Embedded System Designer.
2	**Instruction Sets:** Preliminaries, ARM Processor, TI C55x DSP
3	**CPUs:** Programming Input and Output, Supervisor Mode, Exception and Traps, Co-Processors, Memory System Mechanisms, CPU Performance, CPU Power Consumption, Design Example: Data Compressor
3	**Bus-Based Computer Systems:** The CPU Bus, Memory Devices, I/O Devices, Component Interfacing, Design with Microprocessors, Development and Debugging, System-Level Performance Analysis, Design Example: Alarm Clock
4	**Program Design and Analysis:** Components for Embedded Programs, Models of Program, Assembly, Linking and Loading, Basic Compilation Techniques, Program Optimization
5	**Device Drivers and Interrupt Service Mechanism:** Programmed I/O Busy-Wait Approach without Interrupt Service Mechanism, ISR Concept, Interrupt Sources, Interrupt Servicing (Handling) Mechanism, Multiple Interrupts, Context and the Periods for Context Switching, Interrupt Latency and

	Deadline, Classification of Processors Interrupt Service Mechanism from Context-Saving Angle, Direct Memory Access, Device Driver Programming
6	**Embedded Software Development Process and Tools:** Introduction, Host and Target Machines, Linking and Locating Software, Getting Embedded Software into the Target System, Issues in Hardware-Software Design and Co-design
7	**Testing, Simulation and Debugging Techniques and Tools:** Testing on Host Machine, Simulators, Laboratory Tools

Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand the basics of embedded systems.
- Understand different core components of embedded systems such as hardware, software and I/O devices.
- Understand basic steps and issues in designing of an embedded system.
- Study tools and techniques used in designing and testing of an embedded system.

Books Recommended:-

1. "Embedded Systems – Architecture, Programming and Design", **Raj Kamal**, McGraw Hill
2. "Computer as Components – Principles of Embedded Computing System Design", **Wayne Wolf**, Morgan Kaufman Publishers
3. "Embedded / Real-Time Systems – Conceps Design and Programming – Black Book", **Dr. K. K. V. Prasad**, Dreamtech Press

C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: -Electronics & Communication Engineering
SEMESTER: - I **CODE**: - 5TE01HDL1
NAME – Hardware Description Language (HDL)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE01HDL1	Hardware Description Language (HDL)	04	00	02	06	05	30	1.5	70	3.0	---	20	30	150

Objectives: -

- The objective of the subject is to provide detailed knowledge of Verilog Hardware Description Language, its architectural components and designing examples as well as gate-level synthesis using Verilog HDL

Prerequisites: Basic knowledge of Digital Electronics and Digital Logic Circuits is necessary.

Course Outlines: -

Sr. No.	Course Contents
1	**Introduction to Verilog HDL:** What is Verilog HDL, History, Major Capabilities
2	**A Tutorial:** A Module, Delays, Describing in Dataflow Style, Describing in Behavioral Style, Describing in Structural Style, Describing in Mixed-design Style, Simulating a Design
3	**Language Elements:** Identifiers, Comments, Format, System Tasks and Functions, Compiler Directives, Value Set, Data Types, Parameters
4	**Expressions:** Operands, Operators, Kinds of Expressions
5	**Gate Level Modeling:** Built-in Primitive Gates, Multiple-input Gates, Multiple-output Gates, Tristate Gates, Pull Gates, MOS Switches, Bidirectional Switches, Gate Delays, Array of Instances, Implicit Nets, Examples
6	**User-Defined Primitives:** Defining a UDP, Combinational UDP, Sequential UDP
7	**Dataflow Modeling:** Continuous Assignment, Net Declaration Assignment, Delays, Net Delays, Examples
8	**Behavior Modeling:** Procedure Constructs, Timing Control, Block Statement, Procedure Assignments, Conditional Statement, Case Statement, Loop Statement, Procedural Continuous Assignment
9	**Structural Modeling:** Module, Ports, Module Instantiation, External Ports

10	**Verification:** Writing a Test Bench, Waveform Generation, Testbench Examples, Reading Vectors from a Text File, Writing Vectors to a Text File
11	**Verilog HDL Synthesis –Introduction:** What is Synthesis, Synthesis in a Design Process, Logic Value System, Bit-widths, Value Holders for Hardware Modeling
12	**Verilog Constructs to Gates:** Continuous Assignment Statement, Procedural Assignment Statement, Logical Operators, Arithmetic Operators, Relational Operators, Equality Operators, Shift Operators, Vector Operations, Part-selects, Bit-selects, Conditional Expression, Always Statement, If Statement, Case Statement, More o Inferring Latches, Loop Statement, Modeling Flip-flops

Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand the basics of Verilog Hardware Description Language.
- Understand different architectural components of Verilog HDL, different modeling styles and design examples using Verilog HDL.
- Understand gate-level synthesis using Verilog HDL.

Books Recommended:-

1. "A Verilog HDL Primer", **J. Bhasker**, Star Galaxy Publishing
2. "Verilog HDL Synthesis – A Practical Primer", **J. Bhasker**, Star Galaxy Publishing
3. "Advanced Digital Design with Verilog HDL", **Michael D Ciletti**, PHI
4. "Design through Verilog HDL", **T. Padmanabhan, B. R. Bala Tripura Sundari**, John Wiley
5. "Verilog HDL – A Guide to Digital Design and Synthesis", **Samir Palnitkar**, Pearson

C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: -Technology & Engineering
DEPARTMENT OF: - Electronics & Communication Engineering
SEMESTER: - I **CODE**: -5TE01ADS1
NAME – Advanced Digital System Design (ADS)

Teaching & Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE01ADS1	Advanced Digital System Design (ADS)	04	00	02	06	05	30	1.5	70	3.0	---	20	30	150

Objectives:-

- The objective of this course is to provide focus on both basic principle of digital system design and the use of VHDL in design process. This course also focuses on two types of hardware devices, FPGAs and CPLDs that are widely used to implement digital system designs.

Prerequisites:-

- Understanding of basic electromagnetic wave propagation and characteristics.
- Understanding of basic communications theory.
- Understanding of basic concepts of mechanics and gravitation

Course Outlines:-

Sr. No.	Course Contents
1	**Review of Logic Design Fundamentals:** Combinational Logic, Boolean Algebra and Algebraic Simplification, Karnaugh Maps, Designing with NAND and NOR gates, Hazards in Combinational Networks, Flip-Flops and Latches, Sequential Network Timing, Setup and Hold Times, Synchronous Design, Tristate Logic and Busses.
2	**Designing with Programmable Logic Devices:** Designing with programmable logic devices: Read Only Memory, Introduction to PLA, nMOS logic, NOR-NOR logic Designing with PLA using AND-OR array, Reduced PLA table, Introduction to PAL, Segment of a sequential PAL, Designing with PAL, Logical diagram of 16R4 PAL, Other Sequential PLDs, 22V10 PAL, Output Macrocell
3	**Digital Design with FSM:** State machine modeling: Basics of Moore and Mealy machine, Modeling a Moore FSM (synchronous and asynchronous), Modeling a Mealy FSM (synchronous and asynchronous), Designing with FSM, Interacting state machines
4	**Designing with FPGA and CPLD:** Xilinx 3000 FPGAs architecture-Configurable Memory Cell- Input/Output Blocks-Programmable Interconnects, 4000 series FPGAs architecture- Configurable Memory Cell- Input/Output Blocks, Using a One Hot State Assignment, Altera 7000 series and FLEX 10K series architecture.
5	**Hardware Testing and Testability:** Introduction, Testing Combinational Logic, Testing AND and OR gates for Stuck at Faults, Testing AND-OR Network, Fault Detection using Path Sensitization, Testing Sequential Logic.

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Learning Outcomes:-

This course provides a review of logic design fundamentals. to Satellite communications theory, and the science of mechanics towards the provision of communications and other services using Earth-orbiting satellites. Students completing this course will be able to:

- Identify the fundamentals of orbital mechanics, the characteristics of common orbits used byCommunications and other satellites, and be able to discuss launch methods and technologies.
- Understand the radio propagation channel for Earth station to satellite and satellite to satelliteCommunications links and the basics of designing antenna systems to accommodate the needs of a particular satellite system.
- Be able to calculate an accurate link budget for a satellite or other wireless communications link

Books Recommended:-

1. "Fundamentals of Digital Design", Charles H.Roth,Jr., PWS Pub.Co.,1998.
2. "Digital Design Fundamentals", Kenneth J Breeding, Prentice Hall, Englewood Cliffs, New Jersey.1989.
3. "Circuit Design with VHDL", V.Pedroni, MIT Press, Cambridge, 2004
4. "Digital Systems Testing and Testable Design" – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

Research Reference:-

1. Antennas and Propagation, IEEE Transactions on
2. Communications, IEEE Transactions on
3. Aerospace and Electronic Systems, IEEE Transactions on

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FACULTY OF: - Technology & Engineering
DEPARTMENT OF: -Electronics & Communication Engineering
SEMESTER: - I **CODE**: -5TE01DVD1
NAME – Digital VLSI Design (DVD)

Teaching & Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE01DVD1	Digital VLSI Design (DVD)	04	00	02	06	05	30	1.5	70	3.0	---	20	30	150

Objectives:-

- To enable the students to understand the basic concepts of implementation of digital circuits as a part of application specific IC, by means of basic theoretical concepts along with the implementation in various designing tools.

Prerequisites: -Basic knowledge of Digital logic and Digital circuit particularly at the Gate level is essential. Some experience in programming will be helpful.

Course Outlines: -

Sr. No.	Course Contents
1	**CMOS Inverter:** Basic Circuit and DC Operation – DC Characteristics, Noise Margins, Layout considerations, Inverter Switching Characteristics – Switching Intervals, High-to-Low time, Low-to- High time, Maximum Switching Frequency, Transient Effects on the VTC, RC Delay Modeling, Elmore Delay, Output Capacitance, Inverter Design – DC Design, Transient Design, Driving Large Capacitive Loads.
2	**Switching Properties of MOSFETs:** nMOSFET/ pMOSFET Pass Transistors, Transmission Gate Characteristics, MOSFET Switch Logic, TG-based Switch Logic, D-type Flip-Flop.
3	**Static CMOS Logic Elements:** Complex Logic Functions, CMOS NAND Gate, CMOS NOR Gate, Complex Logic Gates, Exclusive OR and Equivalence Gates, Adder Circuits, Pseudo nMOS Logic Gates, Schmitt Trigger Circuits, SR and D-type Latch, CMOS SRAM Cell, Tri-state Output Circuits.
4	**Power Dissipation in CMOS Digital Circuits:** Dynamic Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Static Power Dissipation – Diode Leakage Current, Subthreshold Leakage Current.
5	**Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families:** Charge Leakage, Charge Sharing, Dynamic RAM Cell, Bootstrapping, Clocked-CMOS, Pre-Charge/ Evaluate Logic, Domino Logic, Multiple-Output Domino Logic, NORA Logic, Single-Phase Logic.

Learning Outcomes:-

- Create a variety of simplified low level schematics of Digital Circuits.
- Students will work more closely with the programming aspects of various designing tools

Books Recommended:-

1. CMOS Digital Integrated Circuits – Analysis and Design, Kang, S. and Leblebici, Y., Tata McGraw Hill (2008) 3rd ed.
2. CMOS VLSI Design: A Circuits and Systems Perspective, Weste, N.H.E. and Eshraghian, K., Addision Wesley (1998) 2nd ed.
3. Digital Integrated Circuits – A Design Perspective, Rabaey, J.M., Chandrakasen, A.P. and Nikolic, B., Pearson Education (2007) 2nd ed.
4. CMOS Circuit Design, Layout and Simulation, Baker, R.J., Lee, H. W. and Boyce, D. E., Wiley - IEEE Press (2004) 2nd ed.

Research Reference:-

1. Emerging and Selected Topics in Circuits and Systems, IEEE Journal
2. Industrial Electronics, IEEE Transactions
3. Solid-State Circuits, IEEE Journal

C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: -Electronics & Communication Engineering
SEMESTER: - I **CODE**: - 5TE01MOS1
NAME – Modern Operating Systems (MOS)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE01MOS1	Modern Operating Systems (MOS)	04	00	02	06	05	30	1.5	70	3.0	---	20	30	150

Objectives: -

- The objective of the subject is to provide detailed knowledge on basics of operating systems, its core architecture and design issues.

Prerequisites: Basic knowledge of Computer hardware and software is necessary.

Course Outlines: -

Sr. No.	Course Contents
1	**Introduction:** What is an Operating System, History, Operating System Zoo, Computer Hardware Review, Operating System Concepts, System Calls, Operating System Structure
2	**Processes and Threads:** Processes, Threads, Inter-process Communication, Classical IPC Problems, Scheduling
3	**Deadlocks:** Resources, Introduction to Deadlocks, The Ostrich Algorithm, Deadlock Detection and Recovery, Deadlock Avoidance, Deadlock Prevention, Other Issues
3	**Memory Management:** Basic Memory Management, Swapping, Virtual Memory, Page Replacement Algorithms
4	**Input/Output:** Principles of I/O Hardware, Principles of I/O Software, I/O Software Layers, Disks, Clocks, Character Oriented Terminals, Graphical User Interfaces, Network Terminals, Power Management
5	**File Systems:** Files, Directories, File System Implementation, Example File Systems
6	**Case Study - UNIX:** Overview of UNIX. Processes in UNIX, Memory Management in UNIX, Input / Output in UNIX, UNIX File System
6	**Introduction to Distributed Systems:** Goals of Distributed System, Hardware and Software Concepts, Design Issues
7	**Communication in Distributed Systems:** Layered Protocols, ATM Networks, Client Server Model, Remote Procedure Call and Group Communication
8	**Synchronization in Distributed Systems:** Clock Synchronization, Mutual Exclusion, E-tech Algorithms, Bully Algorithm, Ring Algorithm, Atomic Transactions

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Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand the basics of operating systems.
- Understand architectural components and functions of operating systems.
- Understand distributed concept in design of an operating system.

Books Recommended:-

1. "Modern Operating Systems", **Andrew S. Tanenbaum**, PHI
2. "Distributed Operating System", **Andrew S. Tanenbaum**, PHI
3. "Embedded Systems – Architecture, Programming and Design", **Raj Kamal**, McGraw Hill
4. "Operating Systems – A Design Oriented Approach", **Charles P. Crowley**, Irwin Publication

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FACULTY OF: - Technology & Engineering
DEPARTMENT OF: -Electronics & Communication Engineering
SEMESTER: - I **CODE**: - 5TE01AMA1
NAME – Advanced Microprocessors Architecture (AMA)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE01AMA1	Advanced Microprocessors Architecture (AMA)	04	00	02	06	05	30	1.5	70	3.0	---	20	30	150

Objectives: -

- The objective of the subject is to provide detailed knowledge on advanced microprocessors like AVR and ARM used in design of embedded systems.

Prerequisites: Basic knowledge of microprocessor, microcontroller and assembly as well as c programming is necessary.

Course Outlines: -

Sr. No.	Course Contents
1	**AVR RISC Architecture:** AVR Family Architecture, Register File, ALU, Memory Access and Instruction Execution, I/O Memory, EEPROM, I/O Ports, SRAM, Timer, UART, Interrupt Structure, Internal Watchdog Timer, Power-Down Modes of Operation, Types of AVR Controllers
2	**AVR Instruction Set:** Program and Data Addressing Modes, Arithmetic and Logical Instructions, Program Control Instructions, Data Transfer Instructions, Bit and Bit-Test Instructions
3	**AVR Hardware Design Issues:** Power Source, Operating Clock Sources, Reset Circuit
4	**Hardware and Software Interfacing with AVR:** A Beginner's Circuit, Lights and Switches, Stack Operation in AVR Processors, Implementing Combinational Logic, Connecting AVR to PC Serial Port, Expanding I/O, Interfacing ADC, Interfacing DAC, Interfacing LED Displays, Interfacing LCD Displays, Driving Relays with AVR, Stepper Motor Interfacing to AVR, Interfacing to Serial EEPROM, Interfacing to RTC, Accessing a Constants Table, Arbitrary Waveform Generation
5	**Communication Links for AVR Processor:** Introduction, RS-232, RS-422/423, RS-485, SPI and MICROWIRE Bus, I2C Bus, PC Parallel Port, ISA, USB, IrDA Data Link, CAN Bus
6	**The ARM Architecture:** The Acorn RISC Machine, Architectural Inheritance, The ARM Programmer's Model, ARM Development Tools
7	**ARM Assembly Language Programming:** Data Processing Instructions, Data Transfer Instructions, Control Flow Instructions,

	Writing Simple Assembly Language Programs
8	**ARM Organization and Implementation:** 3-Stage Pipeline ARM Organization, 5-Stage Pipeline ARM Organization, ARM Instruction Execution
9	**ARM Instruction Set:** Introduction, Exceptions, Conditional Execution, Branch and Branch With Link and With Exchange, Software Interrupt, Data Processing Instructions, Multiply Instructions, Single Word and Unsigned Byte Data Transfer Instructions, Half-Word and Signed Byte Data Transfer Instructions, Multiple Register Transfer Instructions, Swap Memory and Register Instructions (SWP), Status Register to General Register Transfer Instructions, General Register to Status Register Transfer Instructions
10	**Thumb Instruction Set:** Thumb Bit in CPSR, Thumb Programmer's Model, Branch Instruction, Software Interrupt Instruction, Data Processing Instruction, Single Register and Multiple Register Data Transfer Instruction, Breakpoint Instruction, Thumb Implementation, Thumb Applications
11	**ARM7 based Phillips LPC2100 Microcontroller:** Bus Structure, Memory Map, Register Programming, Memory Accelerator Module, Flash Memory Programming, External Bus and Memory Interface, Booting from ROM, Power Control, LPC2000 Interrupt System
12	**LPC2100 User Interface:** General Purpose I/O and Timers, PWM Modulator, RTC, Watchdog Timer, UART, I2C Interfacing, SPI Interfacing, ADC and DAC, CAN Controller

Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand the basics of AVR and ARM microprocessors and RISC architecture.
- Understand architecture, programming and interfacing of AVR and ARM processors
- Understand LPC2100 series microcontroller along with its architecture, programming and interfacing.

Books Recommended:-

1. "Programming and Customizing the AVR Microcontroller", **Dhananjay V. Gadre**, McGraw Hill
2. "ARM System-on-Chip Architecture", **Steve Furber**, Addision Wesley
3. "The Insider's Guide to the Phillips ARM7 based Microcontrollers – An Engineer's Introduction to LPC2100 Series", **Trevor Martin**, Hitex (UK) Ltd.
4. "ARM System Developer's Guide – Designing and Optimizing System Software", **Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield**, Elsevier
5. "The AVR Microcontroller and Embedded Systems using Assembly and C", **Muhammad Ali Mazidi, Sarmad Naimi, Sepehr Naimi**, Prentice Hall - Pearson